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Study on the Performance Improvement of TIPS-Pentacene Transistors with a Nickel Buffer Layer on flexible substrates

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유연한 기판위에 제작된 TIPS-Pentacene 유기 트랜지스터에서 니켈 버퍼층에 의한 성능향상에 관한 연구

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초록: 본 논문에서는 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) 유기 박막 트랜지스터에 니켈 버퍼층을 적층했을 때의 효과를 연구하였다. 니켈(Nickel) / 은(Silver) 소스 드레인 전극은 은 (Silver) 전극이 단독으로 쓰일 때 보다 에너지 레벨차이를 줄여 캐리어의 주입이 더 잘되도록 도와주므로써 전기적 특성을 향상 시켜준다. 또한 유기 게이트 절연체의 추가로 TIPS-pentacene 은 규칙적 배열된 형태를 가지므로써 소자 성능의 향상을 가지고 온다. 제작한 유기박막트랜지스터 에서 0.01 cm^2의 포화영역 이동도를 얻을 수 있었으며, 또한 드레인 전압을 -50 V로 하고 게이트 전압을 20 V에서 -50 V 까지 인가하였을 때 2×10^4의 전멸 비를 얻을 수 있었다. 이러한 결과를 polyethylene terephthalate (PET) 기판을 이용한 유연한 OTFTs에 적용시켜본 결과 유리기판위에 제작했을 때와 비슷한 성능을 얻음을 확인하였다.

Keywords : nickel buffer layer, TIPS-Pentacene FETs, flexible substrate

1. Introduction

Microelectronics has been the technology which development of modern electronic systems, especially in the area of data and signal manipulation. Silicon technology has been the driving force in integrated device manufacturing and is likely to retain this position in the foreseeable future. On the other hand, Organic Thin Film Transistors (OTFTs), which are transistors in which an organic material is used as the active

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semiconductor[1], may form the basis of a new low-cost microelectronic technology on flexible substrates[2]. They guarantee a low process temperature, typically 150 ℃, have low-cost, are unbreakable by impulse, bending or aligning, and enable the simple processing for flexible, and large-area electronic devices[3]. Nevertheless, OTFTs which show the best performance up to date are mostly based on pentacene and gold electrodes with a costly vacuum deposition process. This makes it difficult for OTFTs to move forward and provide the building blocks for low-cost and large-area electronics. However, in solution processing, a functionalized pentacene called 6,13-bis (triisopropylsilylethynyl) pentacene (TIPS-pentacene) has brought about a new prospect[4,5]. In order to fabricate devices which are low cost and have high field-effect mobility, it is essential to the drop casting process to add a Nickel (Ni) buffer layer instead of the existing Gold (Au) source-drain electrodes[6]. In this study, we have demonstrated the effect of the Ni buffer layer, and the source-drain electrodes such as Silver (Ag) do not make as good electric contact with pentacene as Au does[7,8]. Accordingly we have inserted a Ni buffer layer, carriers have to be injected from the Ni layer into the accumulating channel layer through an insulating region of pentacene[9-11]. When the Ni layer is similar to the accumulating channel layer, carriers are directly injected from the Ni layer into the conduction layer. Consequently, we optimized the both drop casting process for TIPS-pentacene on glass substrate and flexible OTFTs applied on polyethylene terephthalate (PET) substrate to achieve a low cost and a high quality electrical performance[12].

2. Experimental

For experiments, devices were first fabricated on glass substrates, which was the bottom-contact structure as shown in Fig. 1. The 100 nm-thick indium-tin-oxide (ITO) as a gate electrode was sputtered onto the substrate and the 200 nm-thick SiO_2 as a gate insulator was deposited by plasma enhanced chemical vapor deposition (PECVD). To improve the quality of interface between organic semiconductor and dielectric, 5 wt% cross-linked poly (4-vinylphenol) (CPVP) in propylens glycol monomethyl ether acetate (PGMEA) was deposited on the SiO_2 as organic-inorganic bi-insulator layer using a spin coating process in a glove box filled with nitrogen gas and them annealed at 165 ℃ for 60 min in a convection oven. The Ni as a buffer layer and the Ag as ource-drain electrodes were deposited onto the CPVP gate insulator through a patterned shadow mask by thermal evaporation at 5×10^{-7} torr and at a thickness of 1 nm and 40 nm-thick, respectively. Finally, the TIPS-pentacene was dropped using a micro-pipette and that filled the gap between source and drain electrode forming a channel layer. For the active layer, 2 wt% of TIPS-pentacene solution in chlorobenzene was prepared and this processing step was done in ambient air. It was then annealed on a hotplate at 60 ℃ for 30 min. In the application to the PET film, 100 nm-thick Al gate electrode was deposited onto the pet substrate with the same condition for preceding Ni and Ag source-drain electrode. After fabricating Al gate electrode, 10wt% CPVP in n-Propanol, to be used as a singe gate insulator, was spin coated in a glove box and then annealed in a vaccum oven at 100 ℃ for 60 minutes[13]. In this study, we used low temperature CPVP because the PET film was damaged at temperatures over 130 ℃. The 1 nm-thick Ni buffer layer and 40 nm-thick Ag source-drain electrodes were deposited by using a thermal evaporator at 5×10^{-7} torr through an identical shadow mask were

deposited with the same manners for former source-drain electrode. Next, the active layer was formed by drop-casting the TIPS-pentacene solution, and this was annealed on a hotplate at 75 °C for 30 min. Thus we made bottom-contact flexible OTFTs on the PET film. With the drop-cast method, expensive machines, such as high-cost vacuum equipment or roll to roll inkjet machines, are unnecessary for producing the active layer. Thus, this method essentially cuts the time and cost of manufacturing the device. The fabricated OTFTs have a channel length of 100 ㎛ and width of 500 ㎛ (W/L=5) respectively. The surface morphology of the proposed devices was observed with atomic force microscopy (AFM, XE-150). The transistor characteristics were measured using a Keithley 4200/semiconductor analyzer in ambient condition.

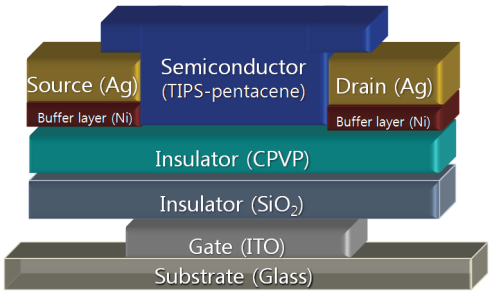

Fig. 1. Structure of a bottom-contact OTFT with a nickel buffer layer.

3. Results and Discussion

The OTFTs with a Ni buffer layer and Ag source-drain electrodes exhibits better performance in comparison with only the Ag source-drain electrodes. The Ni buffer layer is required for the injection of the carrier by direct contact of the electrodes into the conducting channel. Fig. 2 is a plot of the capacitance-frequency (C-F) curves for metal/insulator/metal (MIM) capacitors of the following type at room temperature: Al/ 200-nm-thick SiO_2 as insulator/Al ; Al/370-nm-thick SiO_2/CPVP as a bi-insulator/Al; and Al/490-nm-thick low temperature CPVP as insulator/Al on PET

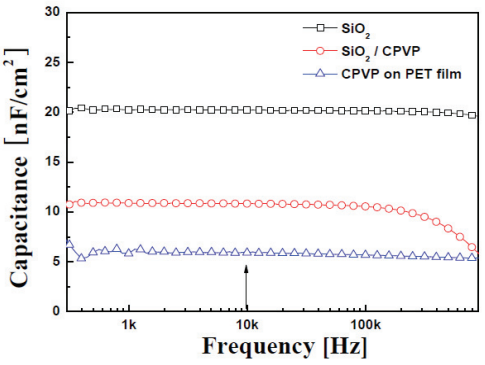

Fig. 2. Comparison of C-F characteristics for the MIM devices fabricated with a various insulator&substrates.

film. The capacitance was 20.21 nF for the SiO_2 layer at 10 KHz, while they were 10.77 nF for the SiO_2 layer and 5.92 nF for the low temperature CPVP insuator for flexible OTFTs at 10 KHz respectively. Fig. 3 shows the electrical characteristics of drop-casted TIPS - pentacene OTFTs. In comparison with the transfer characteristics, it was observed that the Ni buffer layer showed an improved drain current compared to the Ag electrode alone. As shown in Fig. 3 (a) and (b), the best performance from the I_D-V_G curves was observed in TIPS-pentacene TFTs with the Ni buffer layer on the SiO_2/CPVP bi-insulator layer. In this device, on/off current ratio ($I_{on/off}$) is about 2×10^4, the subthreshold slopes are 1.6 V/decade, threshold voltage (V_{th}) is 0 V, the field-effect mobility is 0.014 cm^2/Vs under -50 V gate bias(V_{GS}). V_{GS} = -50 V and 0.014 cm^2/Vs. The field effect mobility (μ_{FET}) is calculated in the saturation region ($V_{Ds} > V_{Gs}-V_T$) from Equation 1.

$$I_{Dsat} = (W/2L)\mu_{FET}C_i(V_{Gs}-V_T)^2 \quad (1)$$

Where, I_{Dsat} is the saturated drain current, W and L are the channel width and length, respectively, and C_i is the capacitance per unit area of the gate dielectric layer. As shown at right side of the Y-axis in Fig. 3 (a) and (b), it was verified that the Ni buffer layer prevens some leakage current flow draining to te gate. Ohmic contact serves to oil the wheels of the carrier injection between the source and drain electrode due to living up the Highest Occupied Molecular Orbital (HOMO) level of TIPS-pentacene and work function of Ag and Ni (Ag = 4.29 eV, Nickel = 5.15 eV)[14]. Not only those, but we also demonstrated carrier injection from the source/drain electrodes to the effective conducting channel in TIPS-pentacene, because of Ni buffer layer's cohesive characteristic[7]. Such excellent adhesion property between gate insulator and source-drain electrodes was obtained with some measurement of contact resistance and surface condition by AFM analysis[15]. The average RMS roughness was 1.01 nm (SiO_2), 0.001 nm (CPVP/SiO_2), 1.161 nm (TIPS-pentacene/SiO_2) and 0.021 nm (TIPS-pentacene/CPVP/SiO_2). From the RMS

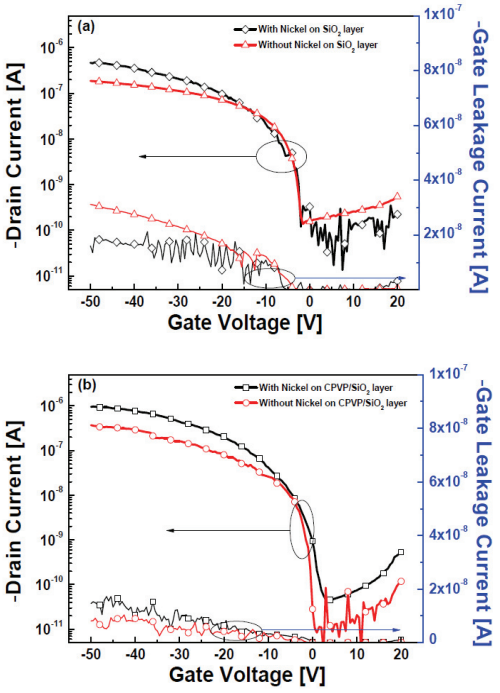

Fig. 3. Transfer characteristics ($\log(-I_D)$ versus V_G) and leakage characteristics (I_G versus V_G) of TIPS-pentacene TFTs:
(a) according to the nickel buffer layer on a SiO_2 layer;
(b) according to the nickel buffer layer on a CPVP/SiO_2 layer.

Table I. The electrical parameters of fabricated TIPS-pentacene TFTs

Insulator	SiO_2/CPVP		SiO_2	
Buffer layer	Ni/Ag	Ag	Ni/Ag	Ag
Threshold voltage [V]	0	2	2	3
Subthreshold slope [V/decade]	1.6	1.6	1.3	1.6
On current [A]	9.54×10^{-7}	4.20×10^{-7}	4.68×10^{-7}	3.28×10^{-7}
Off current [A]	4.44×10^{-11}	2.09×10^{-10}	4.73×10^{-11}	6.61×10^{-10}
On/off ratio	~2.15×10^{4}	~2.01×10^{3}	~9.89×10^{3}	~4.96×10^{2}
Field-Effect Mobility [cm^2/Vs]	1.4×10^{-2}	4.6×10^{-3}	3.1×10^{-3}	1.6×10^{-3}

roughness analysis, it was confirmed that the CPVP/SiO_2 layer showed a relatively smaller RMS roughness than the SiO_2 single layer. It means the inserting of the organic buffer layer had the effect of smoothing the surface of the organic layer compared to the SiO_2 gate dielectric. Thus, the TFTs with an organic gate insulator indicates higher appropriateness for applications to flexible TFTs which need the characteristic of being bendable. Table 1 shows the summarized electrical properties on four kinds of TIPS-pentacene TFTs. Using the Ni buffer layer improves the field effect mobility of about three times than Ag source-drain electrode on a SiO_2 layer. Moreover, the field-effect mobility is also improved about three times when a Ni buffer layer on a SiO_2/CPVP gate insulator layer was located. From the previous study, we applied a Ni buffer layer with a low temperature processed CPVP gate insulator for drop casting processes of TIPS-pentacene on a PET film substrate. Fig. 4 show ID-VD curves on the fabricated flexible OTFTs. From results of the Fig. 4, on/off current ratio is about 1.6×10^4, the sub-threshold slope is 3.2 V/decade, the threshold voltage (V_{th}) is -1 V, and the field-effect mobility is 0.011 cm^2/Vs under V_{GS} of - 50 V.

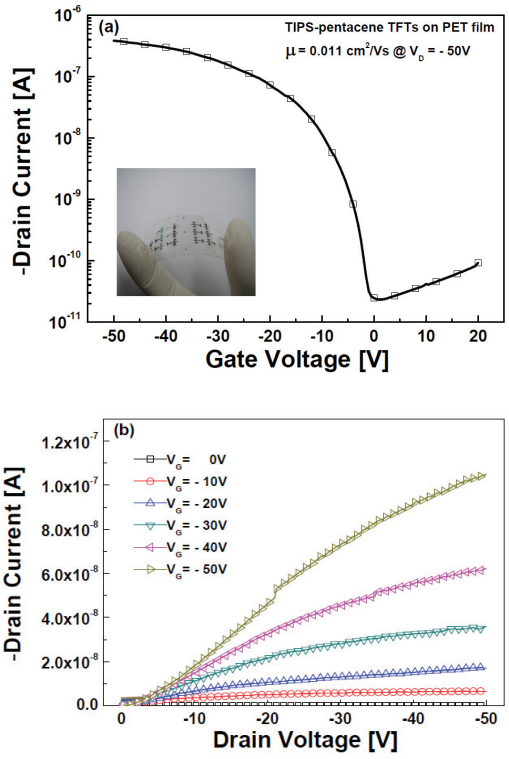

Fig. 4. (a) Transfer characteristics ($\log(-I_D)$ versus V_G) of flexible TIPS-pentacene OTFTs. The inset in the left panel is a photograph of our TIPS-pentacene OTFTs fabricated on PET substrate. (b) Output characteristics (- I_D versus V_D) of flexible TIPS-pentacene OTFTs

4. Conclusions

In this study, we have investigated that the insertion of the Ni buffer layer between Ag source-drain electrode and TIPS-pentacene active layer improves electrical performance in OTFTs. Therefore, we adapted the Ni buffer layer and CPVP gate insulator layer for flexible OTFTs. We fabricated these OTFTs on glass and on PET substrates, respectively, and the compared with each OTFTs. We calculated the field-effect mobility as 0.014 cm^2/Vs for glass and 0.01 cm^2/Vs for the PET substrate. Although these performances need more improvement, our work has lowered the cost compared to method using expensive heat resistant plastic film and fabrication using expensive machines. Such a cost-effective fabrication process could offer the integration of these low cost organic transistors, one of the key goals of which is to achieve an ultra low cost integrated circuit.

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